POWER-UP DETECTION APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a power-up detection apparatus for detecting a time when a power voltage is over a predetermined voltage level, and more specifically, to a power-up detection apparatus configured to perform a stable operation without being affected by power noise.

2. Description of the Related Art

Generally, a power-up detection apparatus initializes a semiconductor device when an externally applied power voltage reaches a predetermined potential. Thereafter, a semiconductor device performs a normal operation when the power voltage is over the predetermined potential.

Fig. 1 shows a circuit diagram of a conventional power-up detection apparatus.

The conventional power-up detection apparatus comprises a voltage divider 1, a potential detector 2, an inverter INV1, and a buffer 3. The voltage divider 1 divides a power voltage VCC in a predetermined ratio. The potential detector 2 compares a predetermined potential with a potential N0 outputted from the voltage divider 1,

and then outputs a comparison result N1. The inverter INV1 inverts the potential N1 detected by the potential detector 2. The buffer 3 buffers an output signal N2 of the inverter INV1 to output a power-up signal PWR.

The voltage divider 1 includes resistors R1 and R2 connected in series between the power voltage VCC and a ground voltage. The divided potential N0 is outputted from a common node of the resistors R1 and R2.

The potential detector 2 includes a resistor R3 and a NMOS transistor NM1. The resistor R3 is connected in series between the power voltage VCC and the ground voltage. The NMOS transistor NM1 has a gate to receive the potential N0 divided by the voltage divider 1. The potential N1 is outputted from a node where the resistor R3 is connected in common to a drain of the NMOS transistor NM1.

The buffer 3 includes inverters INV2 and INV3 for sequentially inverting an output signal N2 from the inverter INV1.

The operation of the conventional power-up detection apparatus is described below.

The power-up detection apparatus detects a potential of an external power voltage VCC, and then generates a power-up signal PWR when the power voltage VCC reaches a predetermined potential.

Here, the power-up signal precharges a predetermined node or circuit to a high or low state for initialization of a chip, that is, for stabilization of an internal power source, until the internal power reaches a predetermined potential.

However, as shown in Fig. 2, if the external power voltage VCC accompanies ripple noise, the state of the power-up signal PWR toggles whenever the power voltage VCC reaches a predetermined potential. As a result, current consumption increases, and mis-operations may occur frequently.

Specifically, as an operation power voltage is lowered, the gap between the operation power potential level and the power potential level where the power-up signal is generated decreases. Accordingly, when noise is generated in the power potential, an undesired power-up signal can be generated, thereby initializing a semiconductor device.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a power-up detection apparatus where a power-up signal is generated only when a potential is maintained over a predetermined level over a predetermined time by

using a time hysteresis device, thereby stably outputting a power-up signal even when a voltage level is unstable or noise is generated.

A power-up detection apparatus is provided comprising a voltage divider, a potential detector and a buffer. The voltage divider divides an inputted power voltage in a predetermined ratio. The potential detector compares a predetermined potential with a potential divided by said voltage divider, and outputs the comparison result. The buffer changes the level of said comparison result when said comparison result outputted from said potential detector is maintained at a predetermined potential for a predetermined period.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a circuit diagram of a conventional power-up detection apparatus.

Fig. 2 is a timing diagram showing the operation of the power-up detection apparatus of Fig. 1.

Fig. 3 shows a circuit diagram of a power-up detection apparatus according to the present invention.

Fig. 4 shows a detailed circuit diagram of a delay unit of Fig. 3.

Fig. 5 is a timing diagram showing the operation of

the power-up detection apparatus of Figs. 3 and 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will be described in detail with reference to the accompanying drawings.

Fig. 3 shows a circuit diagram of a power-up detection apparatus according to the present invention.

The power-up detection apparatus comprises a voltage divider 10, a potential detector 20, an inverter INV11 and a filter unit 30. The voltage divider 10 divides a power voltage VCC in a predetermined ratio. The potential detector 20 compares a predetermined potential with a potential N0 divided by the voltage divider 10, and outputs a comparison result N1. The inverter INV11 inverts a potential N1 detected by the potential detector 20. The filter unit 30 filters an output signal N2 from the inverter INV11, and outputs a power-up signal PWR.

Here, the voltage divider 10 includes resistor R11 and R12 connected in series between the power voltage VCC and a ground voltage. The divided potential N0 is outputted from a common node of the resistors R11 and R12.

The potential detector 20 includes a resistor R13 and a NMOS transistor NM11. The resistor R13 is connected in series between the power voltage VCC and the ground voltage

VSS. The NMOS transistor N11 has a gate to receive the potential N0 outputted from the voltage divider 10. The potential N1 is outputted from a node where the resistor R13 is connected in common to a drain of the NMOS transistor NM11.

The filter unit 30 includes a high filter unit 21 and a low filter unit 22. The high filter unit 21 transits a potential of the power-up signal PWR to a high level only when the potential N2 outputted from the inverter INV11 is maintained at a high level for a predetermined time. The low filter unit 22 transits the potential of the power-up signal PWR to a low level only when the potential N2 outputted from the inverter INV11 is maintained at a low level for a predetermined time.

The high filter unit 21 includes a first delay unit 23 and a NAND gate ND11. The first delay unit 23 delays the output signal N2 of the inverter INV11 for a predetermined time. The NAND gate ND11 NANDs the output signal N2 from the inverter INV11 and an output signal from the first delay unit 23.

The low filter unit 22 includes a second delay unit 24 and a NAND gate ND12. The second delay unit 24 delays an output signal N3 from the high filter unit 21 for a predetermined time. The NAND gate ND12 NANDs the output

signal N3 from the high filter unit 21 and an output signal from the second delay unit 24.

Fig. 4 shows a detailed circuit diagram of the first delay unit 23 of Fig. 3.

The first delay unit 23 includes inverters INV21, INV22, INV23 and INV24, and NAND gates ND21 and ND22. The inverters INV21 and INV22 sequentially invert the output signal from the inverter INV11. The NAND gate ND21 NANDs the output signal N2 from the inverter INV11 and an output signal from the inverter INV22. The inverter INV23 inverts an output signal from the NAND gate ND21. The NAND gate ND22 NANDs the output signal N2 from the inverter INV11 and an output signal from the inverter INV23. The inverter INV24 inverts an output signal from the NAND gate ND22, and outputs an output signal OUT.

Although the NAND gate structure is used herein, various types of delay circuits can be used according to a system or usage.

The second delay unit 24 may have the same structure as that of the first delay unit 23.

Fig. 5 is a timing diagram showing the operation of the power-up detection apparatus of Fig. 3.

When the external power voltage VCC with ripple noise reaches a predetermined potential V1, and it is maintained

over a predetermined potential V1 for a predetermined time, a delay time D of the first delay unit 23, the power-up signal PWR transits to a high level. As a result, the power-up signal PWR does not transits to a high level because the power voltage VCC is not maintained at a high level for a predetermined time D although the power voltage VCC becomes higher than the predetermined voltage V1 for the noise having a short period of high level pulse.

Additionally, the power-up signal PWR does not transits to a low level because the power voltage VCC is not maintained below a predetermined potential V1 for a predetermined time D of the second delay unit 24 although the power voltage VCC becomes lower than the predetermined voltage V1 for the noise having a short period of low level pulse.

The delay time D of each delay unit 23 and 24 is adjustable according to the widths of high or low levels of the noise pulse at the design stage or adjustable by programming when an adjustable delay circuit is used.

As discussed earlier, a disclosed power-up detection apparatus can stably initialize a semiconductor device because a power-up signal is outputted only when an externally inputted power voltage is maintained over a predetermined level over a predetermined period although

the power voltage is affected by noise.